Electronic Version
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Claims

[c1] What is claimed is:

1. A method for generating a high frequency output signal by a plurality of low frequency reference signals, the method comprising:

receiving a plurality of reference signals, wherein a period of each reference signal is identical, a phase difference is predetermined between the reference signals, a signal level of each reference signal in each period fluctuates between a level high and a level low; and

defining the signal level of the output signal as a first level when a number of reference signals belonging to the level high is greater than a number of reference signals belonging to the level low and defining the signal level of an output signal as a second level when a number of reference signals belonging to the level high is smaller than a number of reference signals belonging to the level low, wherein the first level and the second level is non-identical.

[c2] 2. The method of claim 1, wherein the phase difference of the plurality of reference signals is evenly distributed within a corresponding period.

[c3] 3. The method of claim 1, wherein a number of low frequency reference signals is odd.

[c4] 4. The method of claim 1 further comprising:
generating the plurality of reference signals according to a plurality of input signals, the generating a plurality of input signals further comprising:
defining a control signal from one of the input signals and using the rest of the input signals as triggering signals when generating the reference signal, after the control signal changes from the level low to level high but if one of the trigger signals is at level high the reference signals maintain at the level low, after the control signal changes from the level high to level low but if one of the trigger signals is at the level low the reference signals maintain at level high.

[c5] 5. The method of claim 4, wherein generating a plurality of signals comprising:
generating different reference signals by using different input signals among the plurality of input signals.

[c6] 6. The method of claim 4, wherein the plurality of input signals has an identical period but a predetermined phase difference.

[c7] 7. The method of claim 6, wherein the phase difference

between the input signals is evenly distributed within a corresponding period.

[c8] 8. The method of claim 4 further comprising:
generating a plurality of preliminary signals so that the preliminary signals have an identical period but a predetermined phase difference; and
selecting a set of preliminary signals among the plurality of preliminary signals to be the input signals.

[c9] 9. The method of claim 8, wherein a number of preliminary signals is a square of a number of input signals.

[c10] 10. The method of claim 8, wherein the phase difference of the preliminary signals is evenly distributed within a corresponding period.

[c11] 11. The method of claim 4, wherein when generating a plurality reference signals the period of the reference signals is identical to a period of the control signal.

[c12] 12. The method of claim 4 further comprising:
a phase-locked loop (PLL) for generating the plurality of input signals.

[c13] 13. The method of claim 4 further comprising:
a delay-locked loop (DLL) for generating the plurality of input signals.

[c14] 14. A signal circuit comprising:
a frequency multiplication circuit for generating a high frequency output signal by a plurality of low frequency reference signals, the frequency multiplication circuit comprising:
a drive module for generating the output signal according to the plurality of reference signals, wherein a period of the reference signals is identical, a phase difference is predetermined between the reference signals, a signal level of each reference signal in each period fluctuates between a level high and a level low, and for defining the signal level of the output signal as a first level when a number of reference signals belonging to the level high is greater than a number of reference signals belonging to the level low and defining the signal level of the output signal as a second level when a number of reference signals belonging to the level high is smaller than a number of reference signals belonging to the level low, wherein the first level and the second level is non-identical; and
an output terminal electrically connected to the drive module for outputting the output signal.

[c15] 15. The circuit in claim 14, wherein the phase difference of the plurality of reference signals is evenly distributed within a corresponding period.

[c16] 16. The circuit in claim 14, wherein a number of low frequency reference signals is odd.

[c17] 17. The circuit in claim 14, wherein the drive module further comprising:
a plurality of drive circuits corresponding to the reference signals, wherein each drive circuit generate one corresponding reference signal according to a plurality of input signals, each drive circuit comprising:
a plurality of input terminals comprising an input terminal for receiving one input signal as a trigger signal; and
a control terminal for receiving one input signal as a control signal among the plurality of input signals, and for setting the reference signals at level low after the control signal changes from the level low to level high but if one of the trigger signals is at level high and setting the reference signals maintain at the level high after the control signal changes from the level high to level low but if one of the trigger signals is at the level low.

[c18] 18. The circuit in claim 17, wherein the drive circuit receives different input signals as the control signal to generate different reference signals.

[c19] 19. The circuit in claim 17, wherein a period of the plurality of the input signals is identical but a phase differ-

ence between each input signal is predetermined.

[c20] 20. The circuit in claim 19, wherein the phase difference of the inputs signals is evenly distributed within a corresponding period.

[c21] 21. The circuit in claim 17 further comprising:
a phase-locked loop or delay-locked loop for generating a plurality of preliminary signals so that the preliminary signals have an identical period but a different predetermined phase difference and selecting a set of preliminary signals among the plurality of preliminary signals to be the input signals.

[c22] 22. The circuit in claim 21, wherein a number of preliminary signals is a square of a number of input signals.

[c23] 23. The method of claim 21, wherein the phase difference of the preliminary signals is evenly distributed within a corresponding period.

[c24] 24. The method of claim 17, wherein each drive circuit sets the period of the reference signals identical to a period of the control signal.